Soft Error Modeling and Analysis of the Neutron Intercepting Silicon Chip (NISC)

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Introduction

Advances in microelectronic technologies result in semiconductor memories with sub-micrometer transistor dimensions. While the decrease in the dimensions satisfy both the producers' and consumers' requirements, it also leads to a higher susceptibility of the integrated circuit designs to temperature, magnetic interference, power supply and environmental noise, and radiation.

Soft errors are transient circuit errors caused due to excess charge carriers induced primarily by external radiations. The Neutron Intercepting Silicon Chip (NISC) promises an unconventional, portable, power efficient neutron monitoring and detection system by enhancing the soft errors in the semiconductor memories using ^{10}B-enriched regions in the semiconductor memory structure. It was demonstrated that one of the major interferences related to memory devices is soft error or single event upset phenomena and boron content in the Borophosphosilicate glass (BPSG) layers has been proven to be a major source of the soft errors [1-3]. The authors previously published experimental results of soft error rate (SER) dependency on the neutron flux and the operating voltage of the memory and results are used in studies from Intel [4, 5]. ^{10}B-enriched BPSG layers are used to enhance the soft errors by taking advantage of the ^{10}B(n,α[1.47 MeV])^{7}Li[0.84 MeV] reaction. Both of the produced particles have the ability to ionize in the silicon substrate region, which has a comparable thickness with the ranges of these particles.

In this paper, SER simulation results of simple silicon semiconductor memory device node models with different feature sizes and ^{10}B content in the BPSG layers will be presented. An analysis tool is developed for the simulation of the charged particle interactions in the semiconductor memory model, named NISC Soft Error Analysis Tool (NISCSAT). NISCSAT performs the particle transport and tracking via Geant4 [6]. Some features of the NISCSAT are multiple memory node definitions, multiple node layers, multiple source definitions (including cosmic rays and spontaneous fission sources), electromagnetic field support, and detailed records for particles, including the mother particle of the particle that causes the soft error.

NISC Simulation Model

The semiconductor device node represents the basic data storage unit in a semiconductor memory, and for the NISC design it is chosen to be as simple as possible in order to focus on the ^{10}B(n,α)^{7}Li reaction. A cross sectional view of the memory node model is illustrated in Figure 1. The BPSG layer is designed to produce energetic α and ^{7}Li particles, hence it acts as a source for producing soft errors. In a semiconductor memory, depending on the architecture and vendors, there are different layers to produce depletion regions, gates, and isolation layers. Since the objective of this study to focus on feasibility of the NISC, all the actual layers and materials that can be found in a semiconductor memory are lumped into one single region consisting only of silicon. Commercially available semiconductor memory architectures, SRAM, DRAM, and Flash memory have different node architectures and different number of nodes to store a single bit of data, e.g. SRAM can have six transistors while DRAM and Flash memory requires a single transistor to store or the control the storage of the data. However, all of the architectures have a generic structure that can be simplified as a lumped silicon region and a BPSG region that NISC aims to introduce on top of the lumped silicon region.

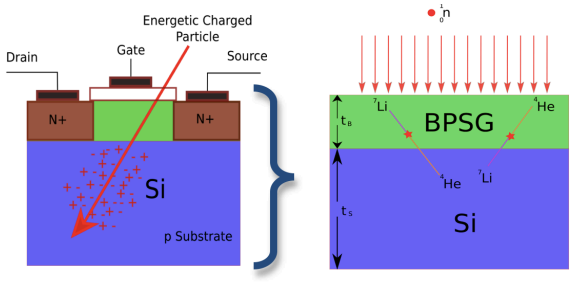

FIGURE 1: Schematic drawing of NISC node model.

Nuclear simulations should be coupled with solid-state device simulations in order to investigate the overall

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system behaviors, including the critical charge of the model and sensitive volume dimensions and locations. The sensitive volume of the node is defined as the induced excess charges in this region most likely cause soft errors and are generally located in the depletion regions that are in close proximity to the gates. The required critical charge depends on the device architecture and operation conditions of the semiconductor memory. However, in this stage these simulations are not coupled with the NISCSAT simulations and reasonable values have been assigned for the critical charge value in the simulations. Generally, critical charge is proportional to the gate interconnects capacitance and voltage, and is therefore sensitive volume thickness. An approximation is used to correlate the critical charge with the sensitive volume thickness length as $Q_{CRIT} \approx 0.0023$ (pC/μm^2) x t^2_S [7,8], where t_S is the thickness of the sensitive volume. This approximation produces reasonable critical charge values and most importantly shows the feature size dependency of the soft errors.

In order to accelerate the convergence and the precision of the Monte Carlo calculations a mono-energetic, mono-directional neutron source is defined on the surface of the memory node and the entire silicon region is assumed as the sensitive volume of the node. Memory node can be treated as a "unit-cell" of the semiconductor memory and can be used to investigate the whole memory soft error analysis. Simulations for single node and node arrays are also performed to observe the applicability of the unit-cell based calculations. Figure 2 illustrates the array structure of the NISC.

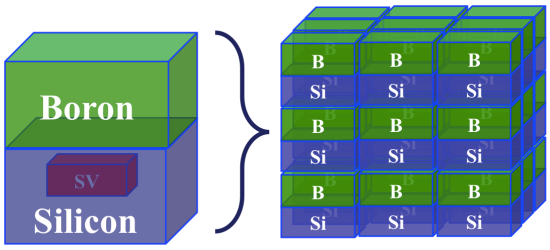

FIGURE 2: Illustration of the NISC array model

Since the main driving mechanism of the NISC is due to the $^{10}B(n,\alpha)^7Li$ reaction, thermal neutron detection is the main consideration but the response of the NISC to fast neutrons is also studied and results are compared with the thermal neutron source calculation results. SER dependency on the BPSG region is investigated with different ^{10}B content in the BPSG region and different node dimensions are used to observe device-scaling effects on the SER. Defined BPSG materials, each having a different ^{10}B content, are given in Table 1. BPSG layer thickness primarily defines the reaction rate probability of the neutrons while the thickness of the Silicon region mainly defines the required critical charge for an upset event in the node for the NISC model.

NISC Simulation Results

NISC node simulations performed with node dimensions of 5 μm x (t_B + t_S) x 5 μm where t_B is the BPSG thickness and t_S is the silicon region thickness. Simulation results with thermal neutrons proved that the SER is proportional to the ^{10}B content of the BPSG region since the reaction probability increases as ^{10}B content increases as given in Figure 3. The solid line represents the boron as the BPSG material and red points represent the compounds, listed in Table 1, as alternative materials for the BPSG material.

TABLE 1: NISC BPSG Materials (NAT: Natural, ENR: Enriched)

Material	Composition (% by weight)	^{10}B Content (%)
B^{NAT}	^{10}B (20), ^{11}B (80)	20
B^{ENR}	^{10}B (90), ^{11}B (10)	90
$BPSG^{NAT}$	$B_2{}^{NAT}O_3$ (15), P_2O_5 (10), SiO_2 (75)	1
$BPSG^{ENR}$	$B_2{}^{ENR}O_3$ (15), P_2O_5 (10), SiO_2 (75)	4
BN^{NAT}	$B^{NAT}N$ (100)	9
BN^{ENR}	$B^{ENR}N$ (100)	39
$B_2O_3{}^{NAT}$	$B_2{}^{NAT}O_3$ (100)	6
$B_2O_3{}^{ENR}$	$B_2{}^{ENR}O_3$ (100)	27

As shown in the Figure 3, there is a neutron self-shielding effect of the boron by increasing ^{10}B content. However, since the neutron mean free path, approximately 20 μm for 90% ^{10}B enriched boron (B^{ENR}), in the boron is much larger than the BPSG thickness, this effect is dominated by the increase in the reaction rates in the BPSG region. Introducing ^{10}B-enriched regions in the NISC increases its detection efficiency of the thermal neutrons by almost two orders of magnitude.

Compounds show similar behavior and due to different interactions of the neutrons and particle ranges in the materials, SER probability slightly differs from the SER probability of the boron.

Device scaling simulations are performed with the thermal neutron source and B^{ENR}; results are given in Figure 4. Enhancement in the soft errors is again observed with increasing ^{10}B. In addition to neutron self-shielding, an increase in the BPSG thickness also

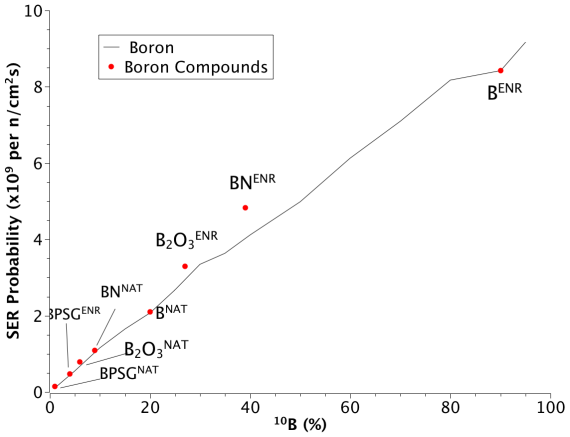

FIGURE 3: Device scaling results for NISC node with B^{ENR} and thermal neutrons.

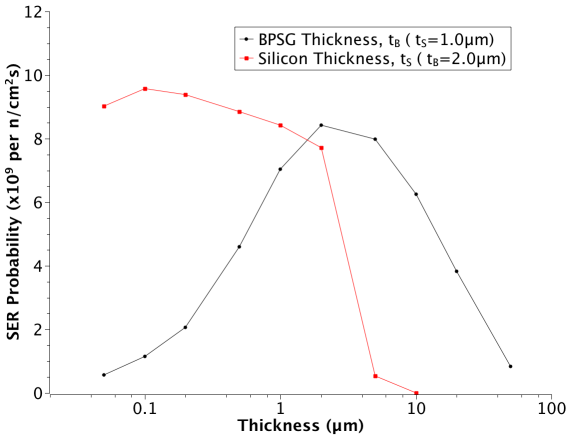

FIGURE 4: Schematic drawing of NISC node model.

shows a self-shielding of α [1.47 MeV] and ^{7}Li [0.84 MeV] particles whose ranges are 3.85 μm and 1.85 μm in the boron. Since α and ^{7}Li particles have almost opposite directions, only one of them contributes to soft error generation in a single node. Therefore, the BPSG layer thickness should not be exceeded much more than the lithium range in the material in order to increase the detection efficiency. Decreasing the silicon thickness means less critical charge is needed and therefore the soft errors increase; however, the reaction probability of the neutrons is also decreased if the BPSG thickness decreases. Therefore, the BPSG thickness should not be decreased as the node dimension decreases in order to get higher efficiencies.

Incoming neutron energy is also proven to be a major component of the SER since the reaction cross section drastically decreases for the fast neutrons, as given in Table 2. Contributions of reactions that can induce soft errors other than $^{10}B(n,\alpha)^{7}Li$ reaction generally have a threshold energy requirement on the incoming neutrons around 4 MeV. Therefore, SER probability is almost zero for the neutron energies above the threshold and can be ignored if compared to thermal neutron results.

TABLE 2: Incoming neutron energy dependency of the NISC. Simulations performed with 5x(2+1)x5 μm node, Q_{CRIT}= 2.3 fC

Neutron Energy	BPSG Material	Soft Errors	
		Source Particles (%)	Node Probability (x10^{9}) per flux (n/cm^{2} s)
0.0253 eV	B^{ENR}	α (65), ^{7}Li (35)	8.43
0.0253 eV	$BPSG^{NAT}$	α (56), ^{7}Li (44)	0.10
2.0 MeV	B^{ENR}	d (100)	0.003
2.0 MeV	$BPSG^{NAT}$	-	-
14 MeV	B^{ENR}	^{10}B (50), ^{25}Mg(50)	0.005
14 MeV	$BPSG^{NAT}$	-	-
50 MeV	B^{ENR}	α (34), ^{28}Si(33), ^{3}He(33)	0.008
50 MeV	$BPSG^{NAT}$	^{28}Si(100)	0.003

In the node calculations, the probability of the multiple bit upsets (MBUs) were ignored since the produced particles that leave the node were killed and cannot contribute SER in another node. However, as given in Figure 5, in the 2D-array of the nodes, MBUs are observed and the increase in the SER probability increases mainly from the alpha particles since they have higher range in the silicon compared to lithium.

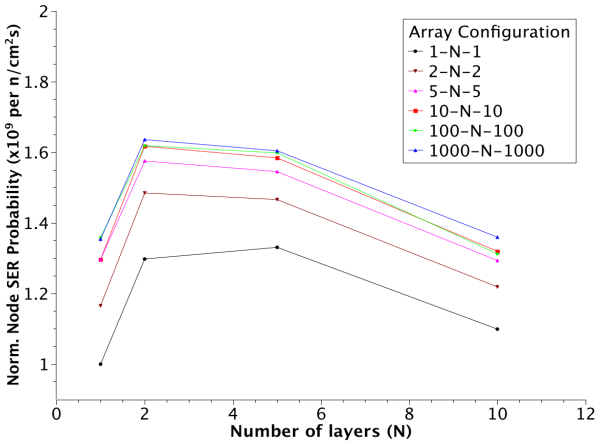

FIGURE 5: Schematic drawing of NISC node model.

In the single node case, the escape probability of one of the particles was high since they have opposite directions and this probability reduces when there is an array of the nodes instead of a single node. In the case of the 3D-array of nodes, the SER probability continues to increase due to MBUs and the contribution of both

particles while the major increase comes from the increase in the neutron reaction rates due to increases in the ^{10}B content at discrete layers. The node SER probability shows a decrease when the total thickness of the layers increases due to self-shielding. However, instead of using one large BPSG layer, which will cause self-shielding, using multi layer memory or multi memory increases SER probability in the overall system.

Summary

This paper briefly summarizes the modeling of the simplified semiconductor memory structure and SER analysis of the NISC node model via neutron interaction simulations using a Geant4 based SER simulation tool, NISCSAT. Simulation results indicated that the NISC can be feasibly applied for thermal neutron detection and monitoring and can be integrated in virtually all semiconductor memory containing commercially available electronic systems. Sensitivity analyses of the NISC with different neutron sources, environmental effects, memory architectures, and cosmic background particles are still in progress. NISCSAT will be integrated with the Soft Error Analysis Tool (SEAT) [9], which supports device level, circuit level, logic level, and architecture level soft error analysis.

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